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EXAMINER	
DICKEY, THOMAS L	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/529,433	Applicant(s) TOUMIYA, YOSHINORI	
	Examiner Thomas L. Dickey	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,18 and 20-22* is/are pending in the application.

4a) Of the above claim(s) *1-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-16,18 and 20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/26/2007 has been entered.

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim 22 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In line 14, "the first and second uppermost wirings" has no antecedent basis. Claim 22 will be examined under the assumption that "the first and second uppermost wirings" relates back to "wirings" introduced in line 3.

Correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 16, 18, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by BENCUYA ET AL. (6,838,715).

Bencuya et al. discloses a solid-state imaging device comprising a plurality of pixels 102 arranged each including a light-receiving portion 308 or 322 and a MOS transistor 108, an Al first uppermost wiring (this is the wiring portion immediately between, and corresponding to, wiring portions 314 and 328. Note that it may be symmetrically disposed with respect to light-receiving portion 314 relative to the un-numbered light-receiving portion, or it may be symmetrically disposed with respect to light-receiving por-

tion 328 relative to light-receiving portion 322, but it cannot be symmetrically disposed relative to both 314 and 328. Wiring portion 314 is offset a distance 372 relative to wiring portion 328. On the other hand, each and every pixel portion 302,304,306 has exactly the same pitch. Note, column 7 lines 47-49, that "It is noted that the positioning and arrangement of photodetectors 308 and 322 and transistor regions 310 and 324 of pixels 302 and 306, respectively, are identical and have a fixed pitch") positioned at a first side of said light-receiving portion 308 or 322; and an Al second uppermost wiring 314 or 328 positioned at an opposite side of said light- receiving portion, the first uppermost wiring and the second uppermost wiring 314 or 328 being_asymmetrically disposed with respect to said light-receiving portion 308 or 322, and a single intra-layer lens 220, 234, etc., formed without being affected by said asymmetrical uppermost wirings and corresponding to each of said light-receiving portions 308 or 322, wherein the center of said intra-layer lens 220, 234, etc., is biased to the center side of an imaging region from the center of said light-receiving portion 308 or 322, when approaching the periphery of the imaging region. Note figures 1A, 1B, 3A, 3B, 4, column 4 lines 7-56, column 6 lines 45-68, and column 7 lines 1-62 of Bencuya et al.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over INOUE ET AL. (6,211,509) in view of Ogawa (6,104,021) and MATSUDA ET AL. (JP11-40787).

Inoue et al. discloses a method for manufacturing a solid-state imaging device comprising the steps of forming wirings 47 on a semi-conductor region 41 in which a plurality of pixels 42-43-44-45 each including a light-receiving portion 42 and a MOS transistor 43 are arranged through an insulation layer 96 with the light-receiving portion 42 in between; wherein uppermost metallic layer wirings 47 are positioned on both sides of said light-receiving portion 42 and asymmetrically disposed with respect to said light-receiving portion 42, and a single intra-layer lens 49 formed without being affected by said asymmetrical uppermost wirings 47 and corresponding to each of said light-receiving portions 42. Note figure 4, column 1, and column 2 lines 1-63 of Inoue et al. Inoue et al. provides a thorough grounding in the type of device Applicants now claim, but Inoue et al. does not disclose the steps of forming a first insulation layer with a first refractive index across the whole surface thereof; and forming a planarizing film with a second refractive index on said first insulation layer to form said single intra-layer lens including said first insulation layer and said planarizing film, or the steps of forming a reflow film with a convexly curved surface at a position corresponding to the respective

light-receiving portions and etching back said reflow film with the first insulation layer to transfer said convexly curved surface onto the first insulation layer.

However, Ogawa discloses a method for manufacturing a solid-state imaging device comprising the steps of forming a first insulation layer 38 with a first refractive index across the whole surface thereof; and forming a planarizing film 53d with a second refractive index on said first insulation layer 38 to form a single intra-layer lens 53 including said first insulation layer 38 and said planarizing film 53d. Note figure 6, column 8 lines 39-67, and column 9 lines 1-38 of Ogawa. Further, Matsuda et al. discloses a method for manufacturing a solid-state imaging device comprising, inter alia, the steps of forming a reflow film 7 with a convexly curved surface at a position corresponding to light-receiving portions and etching back said reflow film 7 with a first insulation layer 6 to transfer said convexly curved surface onto the first insulation layer 6. Note figure 2 and paragraphs 0016-0020 of Matsuda et al. It would further have been obvious to a person having skill in the art to augment Ogawa's method with the steps of forming a reflow film with a convexly curved surface at a position corresponding to light-receiving portions and etching back said reflow film with a first insulation layer to transfer said convexly curved surface onto the first insulation layer, such as taught by Matsuda et al. The Examiner explicitly states (See *KSR International Co. v. Teleflex Inc.,* 550 U. S. __ (2007), slip op. at 14) that there are two reason for combining elements separately

taught in Inoue et al., Ogawa, and Matsuda et al. In the first instance, as Ogawa explains at column 9 lines 39-54:

> When using the buried miniature lens 53, the designer easily optimizes the optical characteristics for the photo diode 31. Because there are various design factors independently changeable, i.e., the ratio of refractive index between the transparent material for the thick layer 38 and the transparent material for the convex lens 53d, the radius of curvature of the surface defining the generally semi-spherical recess 38c, the thickness of the transparent layer 38, the ratio of refractive index between the transparent material for the first transparent layer 53a and the transparent material for the convex lens 53d, the configuration of the curved upper surface 53c and the thickness of each transparent layer 38/53a/53d affect the optical characteristics of the solid state image sensing element 50, and the designer independently changes these factors.

Secondly, it would have made sense to one of skill in the art to augment Ogawa's method with the steps of forming a reflow film with a convexly curved surface at a position corresponding to light-receiving portions and etching back said reflow film with a first insulation layer to transfer said convexly curved surface onto the first insulation layer, such as taught by Matsuda et al. in order to form the interlayer lens in a desired shape with improved condensing efficiency.

B. Claims 12, 13, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over BENCUYA ET AL. (6,838,715) in view of Ogawa (6,104,021).

With regard to claims 12 and 13 Bencuya et al. discloses a method for manufacturing a solid-state imaging device comprising the steps of: forming a plurality of light-receiving portions 308 or 322 on the surface of a substrate 404 (note figure 4) 404; forming first uppermost wiring (this is the wiring portion immediately between, and corresponding to, wiring portions 314 and 328. Note that it may be symmetrically disposed with respect to light-receiving portion 314 relative to the un-numbered light-receiving

portion, or it may be symmetrically disposed with respect to light-receiving portion 328 relative to light-receiving portion 322, but it cannot be symmetrically disposed relative to both 314 and 328. Wiring portion 314 is offset a distance 372 relative to wiring portion 328. On the other hand, each and every pixel portion 302,304,306 has exactly the same pitch. Note, column 7 lines 47-49, that "It is noted that the positioning and arrangement of photodetectors 308 and 322 and transistor regions 310 and 324 of pixels 302 and 306, respectively, are identical and have a fixed pitch") is positioned at a first side of said light-receiving portion 308 or 322; forming a second uppermost wiring 314 or 328 on a second side of the light-receiving portion opposite the first side; the first uppermost wiring not being directly coupled to the second uppermost wiring 314 or 328; wherein the first uppermost wiring and the second uppermost wiring 314 or 328 are asymmetrically disposed with respect to said light-receiving portion 308 or 322, forming a single intra-layer lens 220, 234, etc., without being affected by said asymmetrical first uppermost wiring and second uppermost wiring 314 or 328, and further comprising the steps of: prior to the step of forming said wirings, forming a charge readout transistor 110; forming a gate electrode 310 or 324 to operate said charge readout transistor 110; and forming a planarizing film (described at column 7 lines 21-25 as "a transparent dielectric [not shown in FIG. 3A for ease of illustration] that supports and encapsulates metal one interconnect segments 312 and 326, metal two interconnect segments 314 and 328, and metal three interconnect segments 316 and 330") which covers said gate electrode

310 or 324. Note figures 1A, 1B, 3A, 3B, 4, column 4 lines 7-56, column 6 lines 45-68, and column 7 lines 1-62 of Bencuya et al.

Bencuya et al. does not disclose the steps of forming a first insulation layer having a first refractive index; etching said first insulation layer by using an etching mask and forming a concave portion above said planarizing film over each of said light–receiving portions; and forming a second insulation layer with a second refractive index to bury said concave portion.

However, Ogawa discloses a method for manufacturing a solid-state imaging device comprising the steps of forming a first insulation layer 38 having a first refractive index; etching said first insulation layer 38 by using an etching mask 40 and forming a concave portion 38a above a planarizing film 33c over each of a group of light-receiving portions 31; and forming a second insulation layer 32 with a second refractive index to bury said concave portion 38a. Note figures 3, 4, 5a-c, columns 5-7, and column 8 lines 1-38 of Ogawa. It would have been obvious to a person having skill in the art to modify Bencuya et al.'s method by adding the steps of forming a first insulation layer having a first refractive index; etching said first insulation layer by using an etching mask and forming a concave portion above said planarizing film over each of said light–receiving portions; and forming a second insulation layer with a second refractive index to bury said concave portion, as taught by as taught by Ogawa, thus achieving the claimed invention. The Examiner explicitly states that the reason (See *KSR International Co. v. Teleflex*

Inc., 550 U. S. __ (2007), slip op. at 14) for combining elements separately taught in Bencuya et al. and Ogawa is that, as Ogawa explains at column 9 lines 39-54:

> When using the buried miniature lens 53, the designer easily optimizes the optical characteristics for the photo diode 31. Because there are various design factors independently changeable, i.e., the ratio of refractive index between the transparent material for the thick layer 38 and the transparent material for the convex lens 53d, the radius of curvature of the surface defining the generally semi-spherical recess 38c, the thickness of the transparent layer 38, the ratio of refractive index between the transparent material for the first transparent layer 53a and the transparent material for the convex lens 53d, the configuration of the curved upper surface 53c and the thickness of each transparent layer 38/53a/53d affect the optical characteristics of the solid state image sensing element 50, and the designer independently changes these factors.

With regard to claim 21 Bencuya et al. discloses a method for manufacturing a solid-state imaging device comprising the steps of: forming a first uppermost wiring (this is the wiring portion immediately between, and corresponding to, wiring portions 314 and 328. Note that it may be symmetrically disposed with respect to light-receiving portion 314 relative to the un-numbered light-receiving portion, or it may be symmetrically disposed with respect to light-receiving portion 328 relative to light-receiving portion 322, but it cannot be symmetrically disposed relative to both 314 and 328. Wiring portion 314 is offset a distance 372 relative to wiring portion 328. On the other hand, each and every pixel portion 302,304,306 has exactly the same pitch. Note, column 7 lines 47-49, that "It is noted that the positioning and arrangement of photodetectors 308 and 322 and transistor regions 310 and 324 of pixels 302 and 306, respectively, are identical and have a fixed pitch") positioned at a first side of said light-receiving portion 308 or 322; forming a second uppermost wiring 314 or 328 on a second side of the light-receiving portion opposite the first side; the first uppermost wiring not being directly coupled to the

second uppermost wiring 314 or 328; the first uppermost wiring and the second uppermost wiring 314 or 328 being formed on-a semiconductor region 104 in which a plurality of pixels 102 each including a light-receiving portion 308 or 322 and a MOS transistor 108 are arranged through an insulation layer 305 with the light-receiving portion 308 or 322 in between; and forming a single intra-layer lens 220, 234, etc., wherein a first uppermost wiring portion (this is the wiring portion immediately between, and corresponding to, wiring portions 316 and 330. Note that it may be symmetrically disposed with respect to light-receiving portion 316 relative to the un-numbered light-receiving portion, or it may be symmetrically disposed with respect to light-receiving portion 330 relative to light-receiving portion 322, but it cannot be symmetrically disposed relative to both 316 and 330. Wiring portion 316 is offset a distance 374 relative to wiring portion. On the other hand, each and every pixel portion 302,304,306 has exactly the same pitch. Note, column 7 lines 47-49, that "It is noted that the positioning and arrangement of photodetectors 308 and 322 and transistor regions 310 and 324 of pixels 302 and 306, respectively, are identical and have a fixed pitch") is positioned at a first side of said light-receiving portion and a second uppermost wiring portion 316 or 330 is positioned at an opposite side of said light- receiving portion, the first uppermost wiring portion and the second uppermost wiring portion 316 or 330 being positioned on both sides of said light-receiving portion 308 or 322 and asymmetrically disposed with respect to said light-receiving portion 308 or 322, the first uppermost wiring portion not being directly cou-

pled to the second uppermost wiring portion 316 or 330; wherein said intra-layer lens 220, 234, etc., is formed without being affected by said asymmetrical wirings and corresponding to each of said light-receiving portions 308 or 322. Note figures 1A, 1B, 3A, 3B, 4, column 4 lines 7-56, column 6 lines 45-68, and column 7 lines 1-62 of Bencuya et al.

Bencuya et al. does not disclose the steps of forming a first insulation layer with a first refractive index across the whole surface thereof; selectively removing said first insulation layer with a etching mask by isotropic-etching at a position corresponding to said light-receiving portion to form a concave portion corresponding to each light-receiving portion; forming a second insulation layer with a second refractive index across the whole surface including said concave portion; and planarizing said second insulation layer and making the second insulation layer remain within said concave portion to form the single intra-layer lens from said first and second insulation layers.

However, Ogawa discloses a method for manufacturing a solid-state imaging device comprising the steps of forming a first insulation layer 38 with a first refractive index across the whole surface thereof; selectively removing said first insulation layer 38 with a etching mask 40 by isotropic-etching at a position corresponding to a light-receiving portion to form a concave portion 38a corresponding to each light-receiving portion; forming a second insulation layer 32 with a second refractive index across the whole surface including said concave portion 38a; and planarizing said second insulation layer

32 and making the second insulation layer 32 remain within said concave portion 38a to form a single intra-layer lens 53 comprising said first 38 and second 32 insulation layers. Note figures 3, 4, 5a-c, columns 5-7, and column 8 lines 1-38 of Ogawa. It would have been obvious to a person having skill in the art to modify Bencuya et al.'s method by adding the steps of forming a first insulation layer with a first refractive index across the whole surface thereof; selectively removing said first insulation layer with a etching mask by isotropic-etching at a position corresponding to said light-receiving portion to form a concave portion corresponding to each light-receiving portion; forming a second insulation layer with a second refractive index across the whole surface including said concave portion; and planarizing said second insulation layer and making the second insulation layer remain within said concave portion to form the single intra-layer lens from said first and second insulation layers, as taught by Ogawa, thus achieving the claimed invention. The Examiner explicitly states that the reason (See *KSR International Co. v. Teleflex Inc.*, 550 U. S. __ (2007), slip op. at 14) for combining elements separately taught in Bencuya et al. and Ogawa is that, as Ogawa explains at column 9 lines 39-54:

> When using the buried miniature lens 53, the designer easily optimizes the optical characteristics for the photo diode 31. Because there are various design factors independently changeable, i.e., the ratio of refractive index between the transparent material for the thick layer 38 and the transparent material for the convex lens 53d, the radius of curvature of the surface defining the generally semi-spherical recess 38c, the thickness of the transparent layer 38, the ratio of refractive index between the transparent material for the first transparent layer 53a and the transparent material for the convex lens 53d, the configuration of the curved upper surface 53c and the thickness of each transparent layer 38/53a/53d affect the optical characteristics of the solid state image sensing element 50, and the designer independently changes these factors.

C. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over BENCUYA ET AL. (6,838,715) in view of Ogawa (6,104,021) and MATSUDA ET AL. (JP11-40787).

Bencuya et al. discloses a method for manufacturing a solid-state imaging device comprising the steps of: forming a plurality of light-receiving portions 308 or 322 on the surface of a substrate 404 (note figure 4) 404; forming a first uppermost wiring (this is the wiring portion immediately between, and corresponding to, wiring portions 314 and 328. Note that it may be symmetrically disposed with respect to light-receiving portion 314 relative to the un-numbered light-receiving portion, or it may be symmetrically disposed with respect to light-receiving portion 328 relative to light-receiving portion 322, but it cannot be symmetrically disposed relative to both 314 and 328. Wiring portion 314 is offset a distance 372 relative to wiring portion 328. On the other hand, each and every pixel portion 302,304,306 has exactly the same pitch. Note, column 7 lines 47-49, that "It is noted that the positioning and arrangement of photodetectors 308 and 322 and transistor regions 310 and 324 of pixels 302 and 306, respectively, are identical and have a fixed pitch") positioned at a first side of said light-receiving portion 308 or 322; forming a second uppermost wiring 314 or 328 on a second side of the light-receiving portion opposite the first side; the first uppermost wiring not being directly coupled to the second uppermost wiring 314 or 328; wherein the first uppermost wiring and the second uppermost wiring 314 or 328 are asymmetrically disposed with respect to said light-

receiving portion 308 or 322, and forming a single intra-layer lens 220, 234, etc., without being affected by said asymmetrical uppermost wirings and corresponding to each of said light-receiving portions 308 or 322. Note figures 1A, 1B, 3A, 3B, 4, column 4 lines 7-56, column 6 lines 45-68, and column 7 lines 1-62 of Bencuya et al.

Bencuya et al. does not disclose the steps of forming a first insulation layer with a first refractive index; forming a second insulation layer with a second refractive index on said first insulation layer; and forming a third insulation layer to cover said convex surface of said first insulation layer prior to the step of forming said second insulation layer, or the steps of forming a reflow film with a convexly curved surface at a position corresponding to the respective light-receiving portions and etching back said reflow film with the first insulation layer to transfer said convexly curved surface onto the first insulation layer.

However, Ogawa discloses a method for manufacturing a solid-state imaging device comprising the steps of forming a first insulation layer 38 with a first refractive index; forming a second insulation layer 53d with a second refractive index on said first insulation layer 38; and forming a third insulation layer 53a to cover said convex surface of said first insulation layer 38 prior to the step of forming said second insulation layer 53d. Note figure 6, column 8 lines 39-67, and column 9 lines 1-38 of Ogawa. Further, Matsuda et al. discloses a method for manufacturing a solid-state imaging device comprising, inter alia, the steps of forming a reflow film 7 with a convexly curved surface at a

position corresponding to light-receiving portions and etching back said reflow film 7 with a first insulation layer 6 to transfer said convexly curved surface onto the first insulation layer 6. Note figure 2 and paragraphs 0016-0020 of Matsuda et al. It would further have been obvious to a person having skill in the art to augment Ogawa's method with the steps of forming a reflow film with a convexly curved surface at a position corresponding to light-receiving portions and etching back said reflow film with a first insulation layer to transfer said convexly curved surface onto the first insulation layer, such as taught by Matsuda et al. The Examiner explicitly states (See *KSR International Co. v. Teleflex Inc.,* 550 U. S. __ (2007), slip op. at 14) that there are two reason for combining elements separately taught in Bencuya et al., Ogawa, and Matsuda et al. In the first instance, as Ogawa explains at column 9 lines 39-54:

> When using the buried miniature lens 53, the designer easily optimizes the optical characteristics for the photo diode 31. Because there are various design factors independently changeable, i.e., the ratio of refractive index between the transparent material for the thick layer 38 and the transparent material for the convex lens 53d, the radius of curvature of the surface defining the generally semi-spherical recess 38c, the thickness of the transparent layer 38, the ratio of refractive index between the transparent material for the first transparent layer 53a and the transparent material for the convex lens 53d, the configuration of the curved upper surface 53c and the thickness of each transparent layer 38/53a/53d affect the optical characteristics of the solid state image sensing element 50, and the designer independently changes these factors.

Secondly, it would have made sense to one of skill in the art to augment Ogawa's method with the steps of forming a reflow film with a convexly curved surface at a position corresponding to light-receiving portions and etching back said reflow film with a first insulation layer to transfer said convexly curved surface onto the first insulation

layer, such as taught by Matsuda et al. in order to form the interlayer lens in a desired shape with improved condensing efficiency.

Response to Arguments

5. Applicant's arguments with respect to claims 12-16, 18, and 20-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access

to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thomas L. Dickey/
Primary Examiner
Art Unit 2826